ABSTRACT

LATCH CIRCUIT CAPABLE OF ENSURING RACE-FREE STAGING FOR SIGNALS IN DYNAMIC LOGIC CIRCUITS

A latch circuit capable of ensuring race-free staging for signals in dynamic logic circuits is disclosed. The latch circuit includes four separate logic gates. The first inputs of the first and second logic gates are connected to a first and second precharged internal nodes of the dynamic logic circuit, respectively. The second inputs of the first and second gates are connected to a first and second differential outputs of the dynamic logic circuit, respectively. The first inputs of the third and fourth gates are connected to an output of the first and second logic gates, respectively. The second input of the fourth gate is connected to an output of the third logic gate to provide a first output for the latch circuit. Similarly, the second input of the third logic gate is connected to the output of the fourth logic gate to provide a second output for the latch circuit.